JP INFOTECH

2018 - 2019 VLSI IEEE FINAL YEAR Projects @ JP iNFOTeCH

S.NO	Project Code	IEEE 2018-19 VLSI Project Titles	Tool
		LOW POWER	
1	JPV1801	A 0.9-V 12-bit 100-MS/s 14.6-fJ/Conversion-Step SAR ADC in 40-nm CMOS	TANNER
2	JPV1802	A 128-Tap Highly Tunable CMOS IF Finite Impulse Response Filter for Pulsed Radar Applications	TANNER
3	JPV1803	A Reconfigurable LDPC Decoder Optimized for 802.11n/ac Applications	XILINX
4	JPV1804	Approximate Sum-of-Products Designs Based on Distributed Arithmetic	XILINX
5	-	-	-
6	JPV1806	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates	TANNER
7	JPV1807	SRAM Circuits for True Random Number Generation Using Intrinsic Bit Instability	TANNER
8	JPV1808	The Implementation of the Improved OMP for AIC Reconstruction Based on Parallel Index Selection	TANNER
		HIGH SPEED DATA TRANSMISSION	
9	JPV1809	A 12-bit 40-MS/s SAR ADC With a Fast-Binary-Window DAC Switching Scheme	TANNER
10	JPV1810	A 3.2-GHz Supply Noise-Insensitive PLL Using a Gate-Voltage-Boosted Source-Follower Regulator and Residual Noise Cancellation	XILINX
11	JPV1811	A Fast-Locking, Low-Jitter Pulsewidth Control Loop for High-Speed ADC	TANNER
12	JPV1812	A High-Accuracy Programmable Pulse Generator With a 10-ps Timing Resolution	XILINX
13	JPV1813	A Variable-Size FFT Hardware Accelerator Based on Matrix Transposition	XILINX
14	JPV1814	Algorithm and VLSI Architecture Design of Proportionate-Type LMS Adaptive Filters for Sparse System Identification	XILINX
15	JPV1815	Combating Data Leakage Trojans in Commercial and ASIC Applications With Time-Division Multiplexing and Random Encoding	XILINX
16	JPV1816	Low Phase Noise Ku-Band VCO With Optimal Switched-Capacitor Bank Design	TANNER

17	JPV1817	Low-Complexity VLSI Design of Large Integer Multipliers for Fully Homomorphic Encryption	XILINX
18	JPV1818	Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add	XILINX
AREA EFFICIENT/ TIMING & DELAY REDUCTION			
19	JPV1819	A 588-Gb/s LDPC Decoder Based on Finite-Alphabet Message Passing	XILINX
20	JPV1820	An Efficient Fault-Tolerance Design for Integer Parallel Matrix–Vector Multiplications	XILINX
21	JPV1821	Analysis and Design of Cost-Effective, High-Throughput LDPC Decoders	XILINX
22	JPV1822	Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers	XILINX
23	JPV1823	Basic-Set Trellis Min–Max Decoder Architecture for Non binary LDPC Codes With High-Order Galois Fields	XILINX
24	JPV1824	Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction	XILINX
25	JPV1825	Fast Neural Network Training on FPGA Using Quasi-Newton Optimization Method	XILINX
26	JPV1826	Feedback-Based Low-Power Soft-Error-Tolerant Design for Dual-Modular Redundancy	XILINX
27	JPV1827	Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits	XILINX
Audio, Image and Video Processing			
28	JPV1828	An Energy-Efficient Programmable Many core Accelerator for Personalized Biomedical Applications	XILINX
29	JPV1829	VLSI Design of an ML-Based Power-Efficient Motion Estimation Controller for Intelligent Mobile Systems	XILINX

PROJECT SUPPORT TO REGISTERED STUDENTS:

1) IEEE Base paper.

2) Abstract Document.

3) Future Enhancement (based on Requirement).

4) Modified Title / Modified Abstract (based on Requirement).

5) Complete Source Code/Simulation File/ Hardware Kit.

6) How to Run execution help file.

7) Software Packages

8) International Conference / International Journal Publication based on your project.

OUR OTHER SALIENT FEATURES:

- Number 1 Project Master in Pondicherry/Puducherry
- Guided more than 50,000 students.
- Successfully conducted more than 25 International Conferences in all over South India from 2013 to 2018.
- For the academic year **2018- 2019**, we have Signed MoU with Many Engineering Colleges in all over India to Conduct International Conferences in academic year 2018 – 2019, Where the Registered Students of JP INFOTECH, can easily publish their Project Papers.
- Published more than 5000 Research Articles of Our Ph.D./M.Phil/ME/M.Tech./BE/B.Tech. Students in Leading International Conferences and International Journals from 2013 to 2018.
- From the year **2013 to 2018,** we are Recognized and Awarded from the following colleges: "Paavai College of Engg", "Arjun College of Technology", "K.S.R. College of Engineering", "Vetri Vinayaha College Of Engineering And Technology", "SKR Engineering College", "Sree Sastha Institute of Engineering and Technology", "Jaya Engineering College", "V.P.Muthaiah Pillai Meenakshi Ammal Engineering College for Women", "Muthayammal Arts and Science College", "Sri Raaja Raajan College of Engineering and Technology", "Latha Mathavan Engineering College", "Dr Pauls Engineering College", "Jain College of Engineering", "Manakula Vinayagar Institute of Technology", "CK College of Engineering & Technology" etc.

- Recognized and published article about JP INFOTECH and its director in "THE HINDU", "DINAKARAN" and many more newspapers and Media.
- Leaders with more than 9+ years of experience
- We assist and guarantee you to publish a paper on your project in INTERNATIONAL JOURNAL PUBLICATIONS / INTERNATIONAL CONFERENCE PUBLICATIONS.
- No False Promises.
- 100% Assurance for Project Execution.
- 100% LIVE EXPLANATION
- VALID TRAINEE CERTIFICATION (ISO Certification)
- 100% PLACEMENT SUPPORT
- Own Projects are also welcomed.

So don't wait any more!!! Join us and be a part of us. Walk-in to our Office OR E-mail us your requirements and Register your projects.

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